UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/887,925	06/22/2001	Aniruddha P. Joshi	42390.P11393	7464

7590 02/26/2004

Edwin H. Taylor
Blakely, Sokoloff, Taylor & Zafman LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025-1030

EXAMINER	
VU, TRISHA U	

ART UNIT	PAPER NUMBER
2112	2

DATE MAILED: 02/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/887,925	JOSHI ET AL.	
	Examiner	Art Unit	
	Trisha U. Vu	2112	

-- The MAILING DATE of this c mmunication appears on the cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 are presented for examination.

Claim Objections

2. Claim 1 is objected to because of the following informalities: "being couple" (line 4) should be changed to "being coupled". Appropriate correction is required.

3. Claim 10 is objected to because of the following informalities: "are" (line 1) should be changed to "is". Appropriate correction is required.

4. Claim 16 is objected to because of the following informalities: "is" (line 4) should be changed to "in". Appropriate correction is required.

5. Claim 19 is objected to because of the following informalities: "an data bus" (line 2) should be changed to "a data bus". Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-5 and 7-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Michael (5,787,306).

As to claim 1, Michael teaches a computer peripheral device comprising: a memory (register 30) for storing a configuration address (col. 3, lines 57-62); and a

power level control circuit for controlling the power level in the device (since when the system is powered down, the address stored in the device is lost, it is inherent that there is a power level control circuit in the device to receive power from the system) (col. 4, lines 44-47), the circuit being coupled to the memory to cause the memory to store the configuration address from a bus when the device enters a normal power mode (upon powered up) (col. 3, lines 28-67).

As to claims 2-3, Michael further teaches the memory once storing a configuration address, retains that address until the device is reset or power is turned on or off, and the memory device does not change its stored address when the device is reconfigured (retaining the address of the device and configuring the address again each time the system is powered up) (col. 6, lines 35-40).

As to claim 4, Michael further teaches the bus is an address bus (col. 2, lines 26-29).

As to claims 5 and 7, Michael further teaches the memory restores an address after a reset signal is received by the circuit or power is turned on or off (Fig. 4, and col. 6, lines 35-40).

As to claim 8, Michael teaches a computer system comprising: a processor (CPU 22); and a plurality of peripheral devices (devices 1-n) coupled to the processor through at least one bus (Figs. 1 and 3), each device having a power level control circuit (since when the system is powered down, the address stored in the device is lost, it is inherent that there is a power level control circuit in the device to receive power from the system) (col. 4, lines 44-47) and storage circuit (register 30) for storing a configuration address

(col. 3, lines 57-62), the storage circuit storing a configuration address from the bus when the power level control circuit initially powers up the device in a normal operating mode (upon powered up) (col. 3, lines 28-67).

As to claim 9, Michael further teaches the bus is an address bus (col. 2, lines 26-29).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Michael (5,787,306) as applied to claim 5 above, and further in view of Applicant's Admitted Prior Art (hereinafter AAPA).

As to claim 6, Michael does not explicitly disclose the circuit is responsive to two addresses once a configuration address is stored. AAPA teaches peripheral devices which are responsive to two addresses (two addresses are required for operation of the peripheral device in most instances such as for SIO) (page 2, paragraph [0004] and page 6, paragraph [0013]). It would have been obvious to one of ordinary skill in the art to include peripheral devices responsive to two addresses as taught by AAPA in the system of Michael to allow operation of peripheral devices such as SIO.

8. Claims 10-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Michael (5,787,306) in view of Amin et al. (6,429,706) (hereinafter Amin).

As to claim 10, the argument above for claim 8 applies. However, Michael does not explicitly disclose each of the peripheral devices is initially sequentially brought into a normal operating mode from a stand by mode. Amin teaches each of the peripheral devices is initially sequentially brought into a normal operating mode from a stand by mode (sequentially power up each device) (col. 1, lines 34-41 and 58-67). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement sequentially bring each of the peripheral devices into a normal operating mode from a stand by mode as taught by Amin in the system of Michael to avoid potentially damaging power spikes (col. 1, lines 34-41).

As to claim 11, Amin further teaches the peripheral devices are sequentially powered up after a reset or after power is turned on or off (col. 3, lines 40-45).

As to claim 12, Michael teaches a computer system comprising: a processor (CPU 22); an output unit (power unit) coupled to the processor (it is inherent that there is a power unit to power up the devices in the system) (col. 3, lines 28-30); and a plurality of peripheral devices (devices 1-n) each being coupled to a bus (address bus 10 and/or data bus 12) and each being coupled to a power level control line from the output unit (it is inherent that there is power control line to deliver power to the device to power it up) (Figs 1 and 3), each peripheral device having a memory (register 30) which receives and stores a configuration address from the bus in response to a signal on the power level control line (upon powered up) causing the device to enter a normal operating mode (col.

3, lines 57-62). However, Michael does not explicitly disclose each peripheral device has a separate respective power control line. Amin teaches separate power control line (Fig. 1 and abstract). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement separate power control line for each device as taught by Amin in the system of Michael to allow sequentially powering up each device and thus avoiding potentially damaging power spikes (col. 1, lines 34-41).

As to claim 13, Michael further teaches the bus is coupled between the output unit and the peripheral devices (power is provided between the bus and devices to allow for their communications) (col. 3, lines 28-56).

As to claim 14, Michael further teaches the bus is an address bus (col. 2, lines 26-29).

As to claim 15, Michael further teaches the memory of each of the peripheral devices store a configuration address only when first entering the normal operating mode after a reset or after power is turned on or off (Fig. 4, and col. 6, lines 35-40).

As to claim 16, Michael further teaches storing a unique configuration address in each device as the device enters the normal mode (upon powered up) (col. 3, lines 57-62). However, Michael does not explicitly disclose sequentially entering a normal mode from a standby mode for each peripheral device. Amin further teaches sequentially entering a normal mode from a standby mode for each peripheral device (col. 1, lines 34-41).

As to claim 17, Michael further teaches the storing step occurs after reset (col. 6, lines 35-40).

As to claim 18, Michael further teaches the storing step for each peripheral device includes the reading of data from a bus (col. 6, lines 10-23).

As to claim 19, Michael further teaches the reading of data from a bus comprises the reading of data from a data bus (key code on the data bus 12) and an address from an address bus (address on address bus 10) (col. 6, lines 10-23).

As to claim 20, Michael further teaches configuring each peripheral device after it has stored its configuration address (configuration address is assigned to each peripheral device prior to the device becoming active in the I/O address space) (col. 6, lines 35-47).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, as the art discloses sequentially applying power to devices and/or assigning configuration addresses to devices:

US Patent	6,408,394	Vander Kamp et al.
US Patent	6,594,027	Guillemin et al
US Patent	6,163,823	Henrikson
US Patent	5,974,475	Day et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trisha U. Vu whose telephone number is 703-305-5959. The examiner can normally be reached on Mon-Thur and alternate Fri from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Trisha Vu

Trisha U. Vu
Examiner
Art Unit 2112

uv

Sumati Lefkowitz

SUMATI LEFKOWITZ
PRIMARY EXAMINER